



CJC *IF*
PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

April 6, 2005
Date

Denise Sheridan
Denise Sheridan

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Tongbi Jiang

09,365,356

Attorney Docket No.: 500182.01 (660073.774)

Patent No. : 6,774,480 B1

Issued : August 10, 2004

Title : METHOD AND STRUCTURE FOR MANUFACTURING IMPROVED YIELD
SEMICONDUCTOR PACKAGED DEVICES

NOTIFICATION OF ERRORS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The following errors were noted in a review of the above-identified letters patent. Some of these errors were inadvertently made in the original application, while the others occurred in the printing of the patent. Since the errors are of an obvious nature, a formal Certificate of Correction is not believed to be warranted at this time. Therefore, applicant requests that this notification be placed in the Patent and Trademark Office file.

<u>Column, Line</u>	<u>Reads</u>	<u>Should Read</u>
Column 1, Line 63	"types of packages"	--types of package--
Column 3, Line 51	"package structure"	--package structure.--
Column 4, Line 15	"the substrate 16 may formed"	--the substrate 16 may be formed--

Column 4, Line 47	"skill the art will appreciate in that"	--skill in the art will appreciate that--
Column 7, Line 53	"conductive intrconnect electrically"	--conductive interconnect electrically--
Column 8, Line 11	"the interposer; wherein"	--the interposer wherein--

Respectfully submitted,

Date:

April 4, 2005

By:

Edward W. Bulchis

Edward W. Bulchis, Reg. No. 26,847

Customer No. 27,076

Dorsey & Whitney LLP

1420 Fifth Avenue, Suite 3400

Seattle, WA 98101

(206) 903-8785

Attorneys of Record

EWB:dms

Enclosure:

Postcard